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Anmol Mathur, C. L. Liu

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A Field Programmable Gate Array (FPGA) consists of an array of identical configurable logic blocks (CLBs), each capable of implementing any boolean function with a bounded number of inputs. Such architectural regularity provides an inherent redundancy which can be exploited for fault tolerance and yield enhancement. In this paper we examine the problem of reconfiguring the placement of a circuit on an FPGA to tolerate a given fault pattern in the array of CLBs. The primary objective of the place ...

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5	BRS	L5	0	713/187.ccls. and l1	US- PGPUB; USPAT	2005/07/26 09:00	
6	BRS	L6	0	713/188.ccls. and l1	US- PGPUB; USPAT	2005/07/26 09:00	
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